## AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-39 (Cancelled).

40. (Currently Amended) A semiconductor device comprising:

a semiconductor structure having at least one metal contact formed on a surface thereof;

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact;

a second insulator layer overlying said at least ~~first~~ one metal pad; and,

at least one solder contact formed in the second insulator layer and in contact with said at least one metal pad, said at least one solder contact having a diameter less than 100 microns.

Claims 41-42 (Cancelled).

43. (Currently Amended) The semiconductor device of claim 40, wherein ~~the solder contacts have~~ said at least one solder contact has a diameter less than 10 microns.

44. (Currently Amended) The semiconductor device of claim 40, wherein ~~the solder contacts have~~ said at least one solder contact has a diameter of approximately 2 microns.

45. (Currently Amended) The semiconductor device of claim 40, wherein said at least one metal contact is connected to said at least one metal pad by a via hole formed in the first insulator layer.

46. (Currently Amended) The semiconductor device of claim 40, wherein the at least one solder contact extends from a top surface of the second insulator to the metal pad by a ~~through hole~~ through-hole formed in the second insulator layer.

47. (Original) The semiconductor device of claim 40, wherein the at least one metal pad lies at least partially overtop of the at least one metal contact.

48. (Original) The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit chip.

49. (Original) The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit wafer.

50. (Original) The semiconductor device of claim 40, wherein the semiconductor device is bonded to a module substrate.

51. (Original) The semiconductor device of claim 40, wherein the semiconductor device is bonded to a circuit board.

Claims 52-67 (Cancelled).

68. (Original) The semiconductor device of claim 40, wherein said first insulator layer is at least 2 microns thicker than said at least one metal contact.

69. (Original) The semiconductor device of claim 40, wherein said metal pad comprises a metal stack comprising four different metal levels.

70. (Original) The semiconductor device of claim 69, wherein said metal levels comprise Zirconium, Nickel, Copper and Gold.

71. (Currently Amended) A semiconductor device formed on a semiconductor substrate having at least one metal contact formed thereon, said semiconductor device comprising:

a first ~~insulator~~ insulating layer ~~overlying~~ formed over said at least one metal contact;

at least one metal pad ~~overlying~~ formed over said first ~~insulator~~ insulating layer ~~and in contact with said at least one metal contact~~;

a second ~~insulator~~ insulating layer ~~overlying~~ formed over said at least ~~first~~ one metal pad; and

at least one solder contact formed in the second ~~insulator~~ insulating layer ~~and in contact with said at least one metal pad~~, wherein said at least one solder contact ~~having~~ has a diameter between 2 and 100 microns.

72. (Original) The semiconductor device of claim 71, wherein said at least one solder contact has a diameter of approximately 2 microns.

73. (Cancelled).

74. (Currently Amended) The semiconductor device of claim 40, wherein ~~the solder contacts have~~ said at least one solder contact has a diameter less than 50 microns.

75. (Currently Amended) The semiconductor device of claim 40 wherein ~~the solder contacts have~~ said at least one solder contact has a diameter less than 25 microns.

76. (New) A semiconductor device comprising:

a semiconductor structure having at least one metal layer formed over a surface thereof;

a first insulating layer formed over said at least one metal layer, wherein said first insulating layer is at least two microns thicker than said at least one metal layer;

at least one metal stack formed over said first insulating layer and in contact with said at least one metal layer;

a second insulating layer formed over said at least one metal stack; and,

an etched solder layer having a thickness of at least 2.33 microns, wherein said etched solder layer forms at least one solder contact in said second insulating layer and in contact with said at least one metal stack.

77. (New) The semiconductor device of claim 76, wherein said at least one solder contact has a diameter from 2 microns to 100 microns.

78. (New) The semiconductor device of claim 77, wherein said at least one solder contact has a diameter less than 50 microns.

79. (New) The semiconductor device of claim 78, wherein said at least one solder contact has a diameter less than 25 microns.

80. (New) The semiconductor device of claim 79, wherein said at least one solder contact has a diameter less than 10 microns.

81. (New) The semiconductor device of claim 79, wherein said at least one solder contact has a diameter of approximately 2 microns.

82. (New) The semiconductor device of claim 76, wherein said at least one metal stack is formed of at least three different metals.

83. (New) The semiconductor device of claim 82, wherein said three different metals are zirconium, nickel, and copper.

84. (New) The semiconductor device of claim 82, wherein said at least one metal stack comprises a fourth metal.

85. (New) The semiconductor device of claim 84, wherein said fourth metal is gold.

86. (New) The semiconductor device of claim 76, wherein said second insulating layer is approximately 1.5 microns thick.